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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/898,699	07/02/2001	Dong-woo Lee	9898-176	2435

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EXAMINER	
SINGH, DALIP K	
ART UNIT	**PAPER NUMBER**
2671	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/898,699	LEE ET AL.	
	Examiner	Art Unit	
	Dalip K. Singh	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *2,13,16,19 and 21-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-12,14,15,17,18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendments/RCE

1. This Office Action is in response to applicant's amendment/RCE dated July 12, 2005 in response to PTO Office Action dated May 17, 2005. The amendments to claim(s) 1, 12, 17 and 20; cancellation of claims 2, 13, 16, 19, 21-23 have been noted and entered in the record, and applicant's remarks have been carefully considered resulting in the action as set forth herein below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,758,045 to Moon et al.

a. Regarding claims 1 and 4, Moon et al. **teaches** a memory cell array (Z buffer 81 of a ZDRAM, Fig. 8), a data modifying circuit (a DRAM including a Z value comparator, col. 6, lines 26-35) distinct from the memory controller (memory control logic 72, Fig. 8) adapted to receive corresponding new external depth data from the memory controller (memory control logic 72, Fig. 8), compare the new external depth data with the internal depth data, and write the external depth data in the memory cell array (Z buffer 81 of a ZDRAM, Fig. 8) over the internal depth data depending on the result of the comparison (....two outer pins used in transferring the result of comparison...for decoding a write-signal of memory with receiving the information of comparison result (LT. GT)...the Z buffer, that is, ZDRAM, further comprises...col. 6, lines 36-65) and output to the memory controller (memory control logic 72) a status signal (the outer-control logic 71 decoding

the results 116 of comparison, and the memory control logic 72 receiving the decoded result which is similar to the status signal being outputted to the memory controller (memory control logic 72, Fig. 8, col. 7, lines 25-35)). Claim 4 recites the memory device of claim 1, wherein the data modifying circuit is further adapted to output to the memory controller a status signal, and is not further limiting of the parent independent claim 1.

b. Regarding claim 5, Moon et al. **discloses** use of two outer pins used in transferring the result of comparison (col. 6,lines 26-67). The specification discloses at page 4 lines 10-30 that signals on differ rent pins (control signals CS1/CS2, data I/O pin DQ) are used for providing data flow and logic decisions similar to claim 5 limitation where a status signal is output through the first control pin.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim(s) 3, 6-12, 14, 15, 17, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,758,045 to Moon et al. as applied to claim 1 above, and further in view of U.S. Patent No. 5,301,263 to Dowdell.

a. Regarding claim 3, Moon et al. **discloses** a first control pin (81E, Fig. 9) for receiving a first control signal from the memory controller (memory control logic 72, Fig. 8); and a control circuit (comparator 81A, Fig. 9) for transmitting the external depth data to the memory cell array (81F, Fig. 9). However, Moon et al. **is silent about** bypassing the data modifying circuit depending upon on a state of the first control signal (81E, Fig. 9). The specification describes bypassing the data modifying circuit as an instant where

depth compare writing is not going to occur (...if the first control signal CS1 is in a non-active state,...data NWT is output...for normal writing... Specification page 5, lines 9-21). Dowdell **discloses** similar process as follows in that an incoming z-buffer address, new z-value are given as an entry into FIFO 102. Controller 112 has to act on the incoming pixel address to update the new z-value, **if necessary**. Dowdell makes use of an INVALID bit to validate a new z-value to be written to memory (col. 4, lines 3-67). The most significant, middle significant, and least significant bytes of the old 24 bit z-values, R1, R2 and R3 and corresponding bytes of the new 24 bit z-value denoted by W1, W2 and W3 and a comparison is performed between R1 and W1 and if R1>W1, as determined by the comparator 114, Fig. 2, then it is determined the entire 24 bit old z-value is greater than the entire 24 bit new z-value and consequently the entire 24 bit new z-value consisting of W1, W2 and W3 must be written to memory 124; however, if R1<=W1, then the old 24 bit z-value is less than the new 24 bit z-value, indicating that the new value should not be written to memory and in this case, **the updating operation is terminated** immediately. Other comparisons between R2-W2; R3-W3 are detailed and termination of updating operation is detailed based on the comparisons (col. 4, lines 45-67; col. 5, lines 1-55). Thus INVALID bit state is the signal which then determines bypassing of the update operations. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device as taught by Moon et al. with the feature "bypassing the data modifying circuit by leaving a z-value unchanged based on the INVALID bit and Most significant to least significant bit comparison as detailed above" as taught by Dowdell **because** it results in conserving computing resources as no comparison has to take place.

b. Regarding claims 6 and 7, Moon et al. **does not disclose** a register explicitly for the purpose of storing the received new external depth data. Dowdell's invention

discloses in Fig. 1 a three-step updating operation (i.e., read, compare, write) for a given pixel and a compare circuit (equal comparator 112, greater than comparator 114, Fig. 1, Dowdell). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Moon et al. with the feature "three-step updating operation involving register for storing depth data, comparison circuit for internal/external depth and writing the result based on the comparison" **because** it provides for efficient data processing as z values are updated only if they are determined to be updated and unnecessary processing steps are eliminated resulting in processing efficiencies.

c. Regarding claim 8, Moon et al. **discloses** comparator 81A supplying the comparison results 116 to the outer-control logic 71 which decodes the results 116 and the memory control logic 71 (memory controller) receives the decoded result which is similar to the status signal being outputted to the memory controller (col. 7, lines 10-35).

d. Regarding claims 9-11, Moon et al. **is silent about** wherein the compare circuit compares the internal depth data with the stored external depth in units of X bits/NX bits when the second control signal is in a non-active/active state. Dowdell **discloses** making use of an INVALID bit that indicates for a particular pixel whether or not the corresponding z-value memory location has a valid z-value stored in it, with a value of '0' indicating that it does and a value of '1' indicating that it does not. Further, Dowdell **discloses** most significant, middle significant and least significant bytes of old z-value and new z-value being compared, and this it does not by processing all bits at once. First the MSB are compared, then middle significant and then least significant bytes and avoids unnecessary processing using this logic (see col. 4, lines 40-67; col. 5, lines 1-55) and INVALID bit (value 0 indicating that it does...value 1 indicating it does not...col. 4, lines 3-10), providing a valid status for a z-value at a particular memory location.

Therefore, it would have been obvious to a person of ordinary skill in the art at the invention was made to modify the device as taught by Moon with the "MSB-LSB bit comparison of the old/new z-values in a way that prevents unnecessary logic steps by terminating the updating operation" as taught by Dowdell **because** it results in efficient processing of z-values in the comparator circuit.

e. Regarding claims 12, 14, 15 and 17, Moon et al. **does not disclose** determining a state of the control signal whether active or inactive and comparing the internal/external depth data in units of X/NX bits; and outputting a status signal indicating that the NX bits of the internal depth have been modified. Dowdell **discloses** an INVALID bit which is similar to the control signal with active or inactive states, in that INVALID bit for a particular pixel indicates whether or not the corresponding z-value memory location has a valid z-value stored in it. Dowdell does the 24 bit bits processing for comparing not at once, instead it does so based on MSB-LSB comparison thus avoiding unnecessary comparison steps (col. 4, lines 5-67; col. 5, lines 1-55). Dowdell **does the** reporting of comparison bits and their modification, if carried out, as indicated by "done" state of Fig. 2. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Moon et al. with the feature "MSB-LSB z-bit comparisons and only doing the necessary steps of such comparisons so as to avoid unnecessary logic steps having the z-value bits into MSB-LSB'" as taught by Dowdell **because** it provides for a more efficient z-value comparison logic.

f. Regarding claims 18 and 20, they are similar in scope to claim 5 above and rejected under the same rationale.

Conclusion

4. The following reference, made of record, but not relied upon, is pertinent to z-value bits comparison: U.S. Patent No. 3,955,177 to Miller.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(571) 272-7792**. The examiner can normally be reached on Mon-Friday (10:30AM-6: 30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Ulka Chauhan**, can be reached at **(571) 272-7782**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dalip K. Singh
Examiner, Art Unit 2676

dks
July 23, 2005

ULKA J. CHAUHAN
PRIMARY EXAMINER